PeakTech 12864 LC-Modul

PRODUCT SPECIFICATIONS

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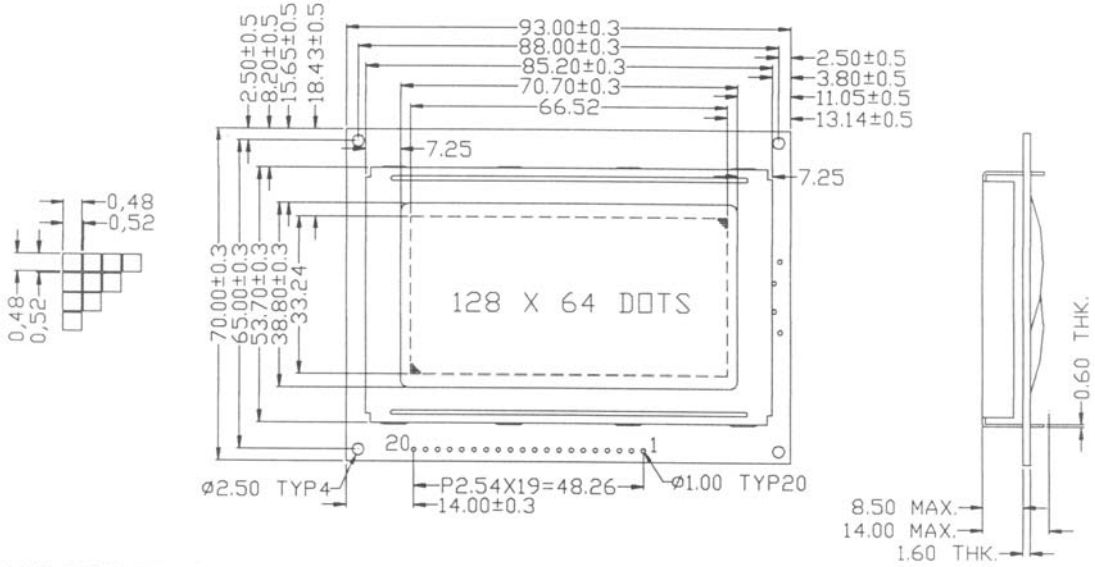
■ PHYSICAL DATA

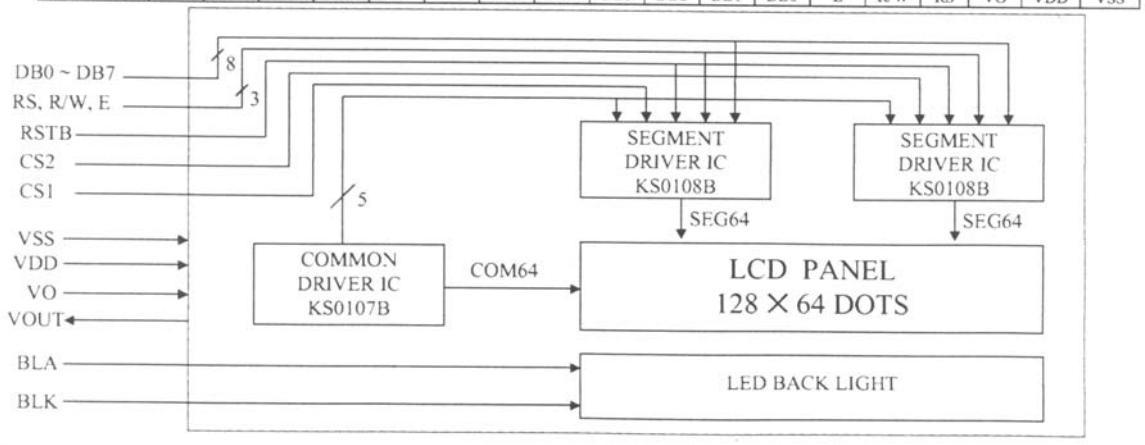
Item	Contents	Unit
LCD type	STN	---
LCD duty	1/64	---
LCD bias	1/9	---
Viewing direction	6	o'clock
Module size (W×H×T)	93 × 70 × 14MAX (3.66″ × 2.76″ × 0.55″MAX)	mm
Viewing area (W×H)	70.7× 38.8 (2.78″ × 1.53″)	mm
Number of dots	128 × 64	dots
Dot size (W×H)	0.48 × 0.48 (0.019″ × 0.019″)	mm
Dot pitch (W×H)	0.52 × 0.52 (0.020″ × 0.020″)	mm

■ EXTERNAL DIMENSIONS



■ BLOCK DIAGRAM

20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
BLK	BLA	VOUT	RSTB	CS2	CS1	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	E	R/W	RS	VO	VDD	VSS



■ ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Parameter	Symbol	Min	Max	Unit
Supply voltage for logic	VDD	-0.3	7.0	V
Supply voltage for LCD	VDD - VO	-0.3	VDD+0.3	V
Input voltage	VI	-0.3	VDD+0.3	V
Operating temperature	TOP	0	50	°C
Storage temperature	TST	-10	60	°C

■ ELECTRICAL CHARACTERISTICS (VDD = +5V±5% , VSS = 0V, Ta = 25°C)

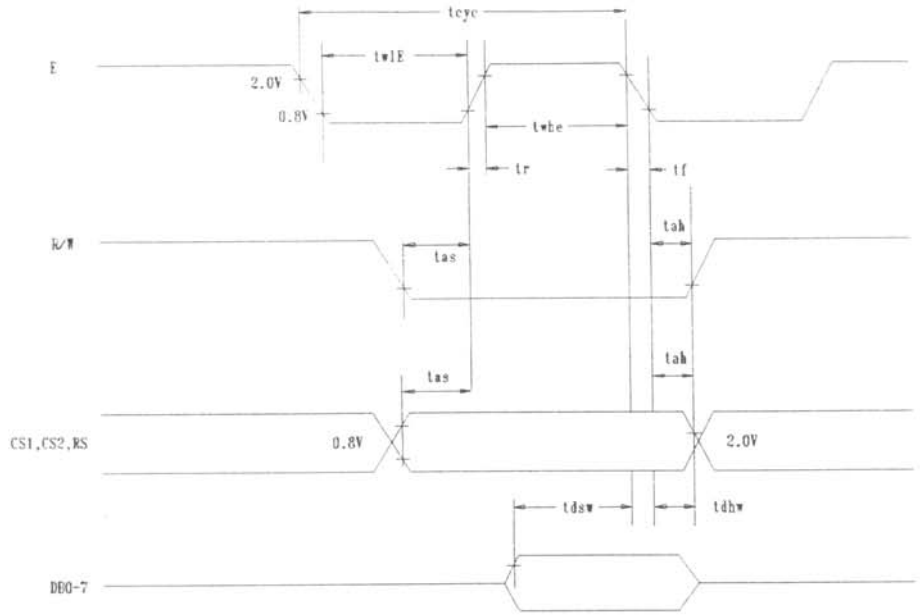
◆ DC Characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Supply voltage for logic	VDD	---	4.5	5.0	5.5	V
Supply current for logic	IDD	---	---	2.02	4	mA
Operating voltage for LCD	VDD - VO	0°C	7.9	8.3	8.7	V
		25°C	7.7	8.1	8.5	V
		50°C	7.5	7.9	8.3	V
Supply voltage for side light	VF	---	---	4.2	4.6	V
Supply current for side light	IF	VF=4.2V	---	160	280	mA
Input voltage ' H ' level	VIH	---	0.7VDD	---	VDD	V
Input voltage ' L ' level	VIL	---	0	---	0.3VDD	V

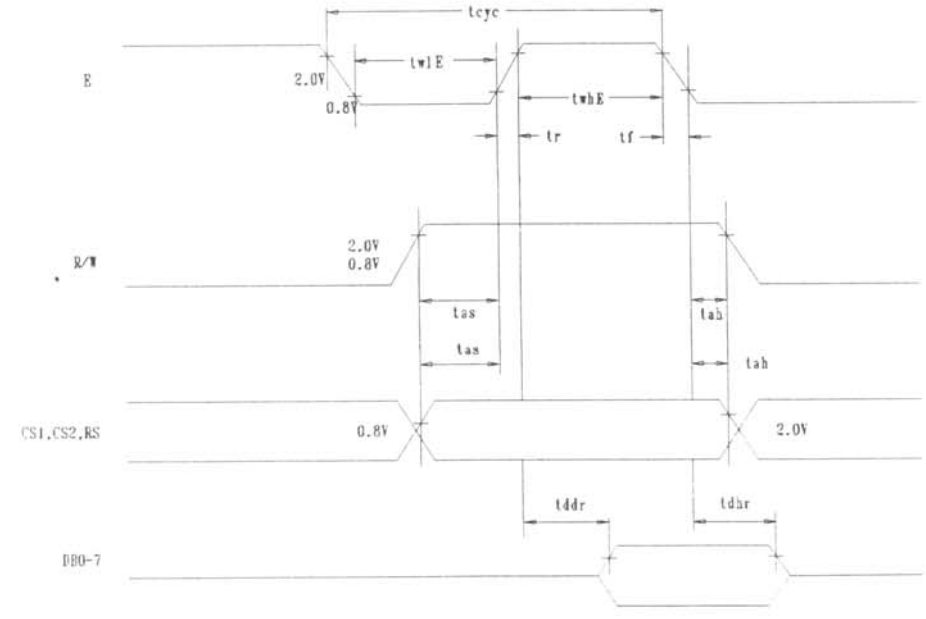
◆ AC Characteristics

● MPU Interface

Characteristic	Symbol	Min	Typ	Max	Unit
E cycle	tcyc	1000	---	---	ns
E high level width	twhE	450	---	---	ns
E low level width	twlE	450	---	---	ns
E rise time	t_r	---	---	25	ns
E fall time	tf	---	---	25	ns
Address set-up time	tas	140	---	---	ns
Address hold time	tah	10	---	---	ns
Data set-up time	tdsw	200	---	---	ns
Data delay time	tddr	---	---	320	ns
Data hold time(write)	tdhw	10	---	---	ns
Data hold time(read)	tdhr	20	---	---	ns



MPU Write Timing



MPU Read Timing

■ OPERATING PRINCIPLES & METHODS

◆ I/O Buffer

Input buffer controls the status between the enable and disable of chip. Unless the CS1 or CS2 is in active mode, input or output of data and instruction do not execute. Therefore internal state is not changed. But RSTB can operate regardless of CS1 and CS2.

◆ Input Register

Input register is provided to interface with MPU which is different operating frequency. Input register stores the data temporarily before writing it into display data RAM.

When CS1 or CS2 is in the active mode, R/W and RS select the input register. The data from MPU is written into input register and then write it into display data RAM. Data is latched when falling of the E signal and written automatically into the display data RAM by internal operation.

◆ Output Register

Output register stores the data temporarily from display data RAM when CS1 or CS2 is in active mode and R/W and RS=H. Stored data in display data RAM is latched in output register. When CS1 or CS2 is in active mode and R/W=H, RS=L, status data (busy check)can be read out.

To read the contents of display data RAM, twice access of read instruction is needed. In first access, data in display data RAM is latched into output register. In second access, MPU can read data which is latched. That is, to read the data in display data RAM, it needs dummy read. But status read does not need dummy read.

RS	R/W	Function
0	0	Instruction
	1	Status read(busy cheek)
1	0	Data write(from input register to display data RAM
	1	Data read(from display data RAM to output register)

◆ Reset

System reset can be initialized by setting RSTB terminal at low level when turning power on, receiving instruction from MPU. When RSTB becomes low, following procedure is occurred.

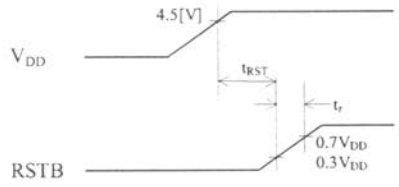
- Display off
- Display start line register become set by 0.(Z-address 0)

While RSTB is low level, no instruction except status read can be accepted. Reset status appears at DB4. After DB4 is low, any instruction can be accepted.

The Conditions of power supply at initial power up are shown in table 1.

Table 1. Power Supply Initial Conditions

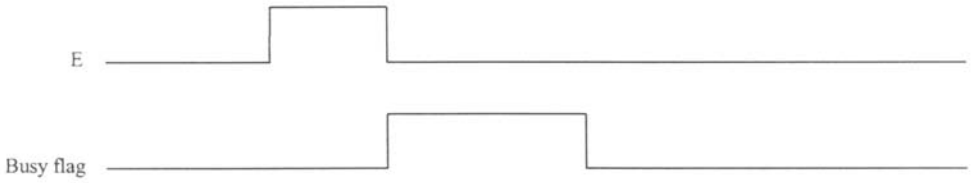
Item	Symbol	Min	Typ	Max	Unit
Reset time	t_{RST}	1.0	---	---	us
Rise time	t_r	---	---	200	ns



◆ Busy Flag

Busy flag indicates that KS0108B is operating or not operating. When busy flag is high, KS0108B is in internal operating. When busy flag is low, KS0108B can accept the data or instruction.

DB7 indicates busy flag of the KS0108B.



◆ Display ON/OFF Flip-Flop

The display on/off flip-flop makes on/off of the liquid crystal display. When flip-flop is reset (logical low). selective voltage or non selective voltage appears on segment output terminals. When flip-flop is set (logical high).non selective voltage appears on segment output terminals regardless of display RAM data.

The display on/off flip-flop can change status by instruction. The display data at all segment disappear while RSTB is low. The status of the flip-flop is output to DB5 by read instruction.

◆ X page Register

X page register designates page of the internal display data RAM. It has not count function. An address is set by instruction.

◆ Y Address Counter

Y address counter designates address of the internal display data RAM. An address is set by instruction and is increased by 1 automatically by read or write operations of display data.

◆ Display Data RAM

Display data RAM stores a display data for liquid crystal display. To express on state of dot matrix of liquid crystal display, write data 1. The other way, off state writes 0.

◆ Display Start Line Register

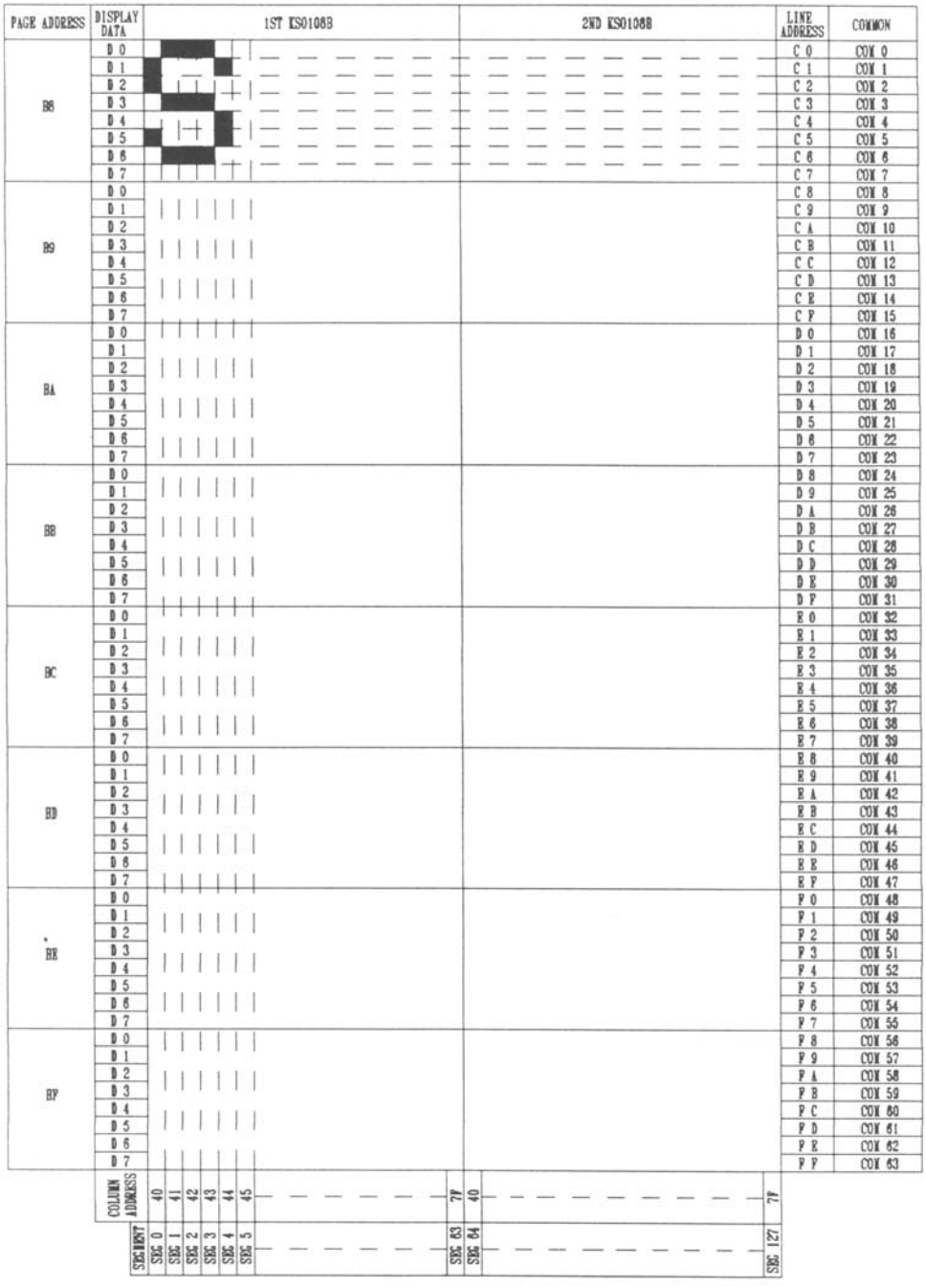
The display start line register indicates address of display data RAM to display top line of liquid crystal display. Bit data (DB<0:5>) of the display start line set instruction is latched in display start line register. It is used for scrolling of the liquid crystal display screen.

◆ Display Control Instruction

The display control instructions control the internal state of the KS0108B. Instruction is received from MPU to KS0108B for the display control. The following table shows various instructions.

Instruction	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Function
Display ON/OFF	0	0	0	0	1	1	1	1	1	0/1	Controls the display on or off. Internal status and display RAM data are not affected. 0:OFF, 1:ON
Set Address	0	0	0	1	Y address (0~63)						Sets the Y address in the Y address counter.
Set Page (X address)	0	0	1	0	1	1	1	Page (0~7)			Sets the X address at the X address register.
Display Start Line	0	0	1	1	Display start line (0~63)						Indicates the display data RAM displayed at the top of the screen.
Status Read	0	1	BUSY	0	ON/OFF	RESET	0	0	0	0	Read status. BUSY 0 : Ready 1 : In operation ON/OFF 0 : Display ON 1 : Display OFF RESET 0 : Normal 1 : Reset
Write Display Data	1	0	Write Data								Writes data (DB0:7) into display data RAM. After writing instruction, Y address is increased by 1 automatically.
Read Display Data	1	1	Read Data								Reads data (DB0:7) from display data RAM to the data bus.

■ DISPLAY DATA RAM ADDRESS MAP



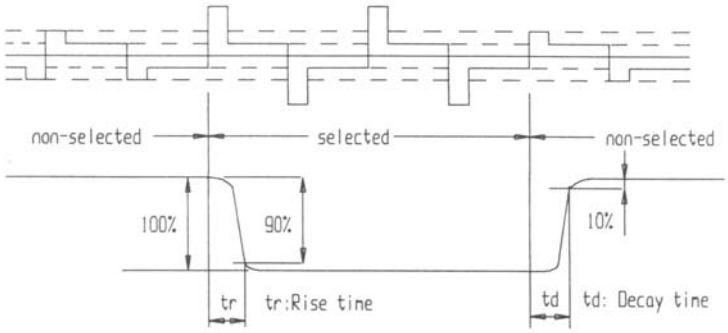
PAGE ADDRESS	DISPLAY DATA	1ST KS0108B	2ND KS0108B	LINE ADDRESS	COMMON
B8	D0			C0	COM 0
	D1			C1	COM 1
	D2			C2	COM 2
	D3			C3	COM 3
	D4			C4	COM 4
	D5			C5	COM 5
	D6			C6	COM 6
	D7			C7	COM 7
B9	D0			C8	COM 8
	D1			C9	COM 9
	D2			CA	COM 10
	D3			CB	COM 11
	D4			CC	COM 12
	D5			CD	COM 13
	D6			CE	COM 14
	D7			CF	COM 15
BA	D0			D0	COM 16
	D1			D1	COM 17
	D2			D2	COM 18
	D3			D3	COM 19
	D4			D4	COM 20
	D5			D5	COM 21
	D6			D6	COM 22
	D7			D7	COM 23
BB	D0			D8	COM 24
	D1			D9	COM 25
	D2			DA	COM 26
	D3			DB	COM 27
	D4			DC	COM 28
	D5			DD	COM 29
	D6			DE	COM 30
	D7			DF	COM 31
BC	D0			E0	COM 32
	D1			E1	COM 33
	D2			E2	COM 34
	D3			E3	COM 35
	D4			E4	COM 36
	D5			E5	COM 37
	D6			E6	COM 38
	D7			E7	COM 39
BD	D0			E8	COM 40
	D1			E9	COM 41
	D2			EA	COM 42
	D3			EB	COM 43
	D4			EC	COM 44
	D5			ED	COM 45
	D6			EE	COM 46
	D7			EF	COM 47
BE	D0			F0	COM 48
	D1			F1	COM 49
	D2			F2	COM 50
	D3			F3	COM 51
	D4			F4	COM 52
	D5			F5	COM 53
	D6			F6	COM 54
	D7			F7	COM 55
BF	D0			F8	COM 56
	D1			F9	COM 57
	D2			FA	COM 58
	D3			FB	COM 59
	D4			FC	COM 60
	D5			FD	COM 61
	D6			FE	COM 62
	D7			FF	COM 63

COLUMN ADDRESS	40	41	42	43	44	45	7F	40	7F
SEGMENT	SEG 0	SEG 1	SEG 2	SEG 3	SEG 4	SEG 5	SEG 63	SEG 64	SEG 127

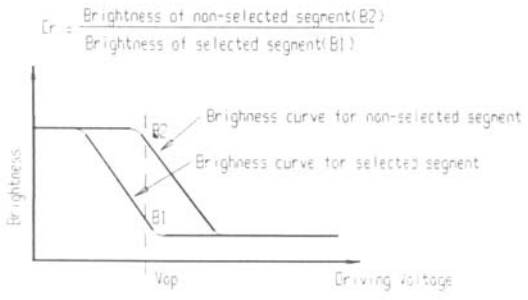
■ ELECTRO-OPTICAL CHARACTERISTICS (V_{OP} = 8.1V, Ta = 25°C)

Item	Symbol	Condition	Min	Typ	Max	Unit	Remarks	Note
Response time	Tr	---	---	332	---	ms	---	1
	Tf	---	---	146	---	ms	---	1
Contrast ratio	Cr	---	---	7.8	---	---	---	2
Viewing angle range	θ	Cr ≥ 2	27	---	---	deg	∅ = 90°	3
			23	---	---	deg	∅ = 270°	3
			30	---	---	deg	∅ = 0°	3
			56	---	---	deg	∅ = 180°	3

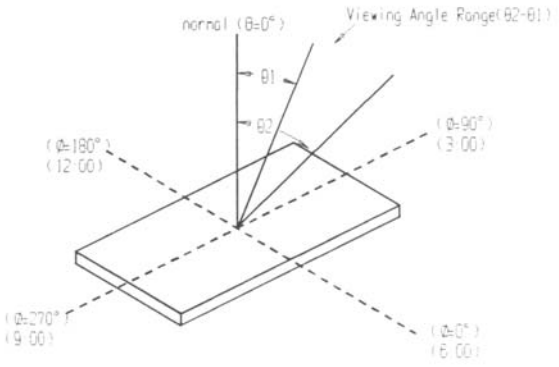
Note1: Definition of response time.



Note2: Definition of contrast ratio 'Cr'.



Note3: Definition of viewing angle.



■ INTERFACE PIN CONNECTIONS

Pin No.	Symbol	Level	Description
1	VSS	0V	Ground
2	VDD	5.0V	Supply voltage for logic
3	VO	---	Input voltage for LCD
4	RS	H/L	H : Data signal, L : Instruction signal
5	R/W	H/L	H : Read mode, L : Write mode
6	E	H, H → L	Chip enable signal
7	DB0	H/L	Data bit 0
8	DB1	H/L	Data bit 1
9	DB2	H/L	Data bit 2
10	DB3	H/L	Data bit 3
11	DB4	H/L	Data bit 4
12	DB5	H/L	Data bit 5
13	DB6	H/L	Data bit 6
14	DB7	H/L	Data bit 7
15	CS1	H	Chip select signal for KS0108B(1)
16	CS2	H	Chip select signal for KS0108B(2)
17	RSTB	L	Reset signal
18	VOUT	-5V	Output voltage for LCD
19	BLA	4.2V	Back light anode
20	BLK	0V	Back light cathode